AMENDED SPECIFICATION

In all representative embodiments presented, the Ge concentration in the source and drain 10 and the SiGe epitaxial channel layer 20 is in the 15% to 50% range, preferably between about 20% to 40%. The SiGe thicknesses in the source/drain 10 are staying below the critical thickness for the given Ge concentration. The critical thickness is defined such that above it the SiGe will relax and defects and dislocations will form. The thickness of the SiGe epitaxial layer 20 typically is between about 5nm and 15nm. The thickness of the epitaxial Si layer 30 is typically between about 5nm and 15nm. Fig. 1A shows an embodiment where the body is bulk Si. These type of devices are the most common devices in present day microelectronics. Figs. 1B and 1C show representative embodiment of the heterojunction source/drain FET device when the Si body 40 is disposed on top of an insulating material 55. This type of technology is commonly referred to as silicon on insulator (SOI) technology. The insulator material 55 usually, and preferably, is SiO_2. Fig. 1B shows an SOI embodiment where the body 40 has enough volume to contain mobile charges. Such SOI devices are called partially depleted devices. Fig. 1C shows an SOI embodiment where the volume of the body 40 is insufficient to contain mobile charges. Such SOI devices are called fully depleted devices. For devices shown in Fig. 1B and 1C there is, at least a thin, layer of body underneath the source and drain 10. This body material serves as the seed material onto which the epitaxial SiGe source and drain 10 are grown. In an alternate embodiment, shown in Fig. 1D, for extremely thin fully depleted SOI devices, one could grow the source and drain 10 laterally, from a lateral seeding, in which case the source and drain 10 would penetrate all the way down to the insulating layer 55.